Getting Started with FPGA Advantage Tutorial

Software Version 5.3

20 June 2002

Copyright © Mentor Graphics Corporation 2000-2002.
All rights reserved.

This document contains information that is proprietary to Mentor Graphics Corporation. The original recipient of this document may duplicate this document in whole or in part for internal business purposes only, provided that this entire notice appears in all copies. In duplicating any part of this document, the recipient agrees to make every reasonable effort to prevent the unauthorized use and distribution of the proprietary information.

This document is for information and instruction purposes. Mentor Graphics reserves the right to make changes in specifications and other information contained in this publication without prior notice, and the reader should, in all cases, consult Mentor Graphics to determine whether any changes have been made.

The terms and conditions governing the sale and licensing of Mentor Graphics products are set forth in written agreements between Mentor Graphics and its customers. No representation or other affirmation of fact contained in this publication shall be deemed to be a warranty or give rise to any liability of Mentor Graphics whatsoever.

MENTOR GRAPHICS MAKES NO WARRANTY OF ANY KIND WITH REGARD TO THIS MATERIAL INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OR MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

MENTOR GRAPHICS SHALL NOT BE LIABLE FOR ANY INCIDENTAL, INDIRECT, SPECIAL, OR CONSEQUENTIAL DAMAGES WHATSOEVER (INCLUDING BUT NOT LIMITED TO LOST PROFITS) ARISING OUT OF OR RELATED TO THIS PUBLICATION OR THE INFORMATION CONTAINED IN IT, EVEN IF MENTOR GRAPHICS CORPORATION HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

RESTRICTED RIGHTS LEGEND 03/97

U.S. Government Restricted Rights. The SOFTWARE and documentation have been developed entirely at private expense and are commercial computer software provided with restricted rights. Use, duplication or disclosure by the U.S. Government or a U.S. Government subcontractor is subject to the restrictions set forth in the license agreement provided with the software pursuant to DFARS 227.7202-3(a) or as set forth in subparagraph (c)(1) and (2) of the Commercial Computer Software - Restricted Rights clause at FAR 52.227-19, as applicable.

Contractor/manufacturer is:
Mentor Graphics Corporation
8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777.

Web site: http://www.fpga-advantage.com
Email: FPGA_support@mentor.com

This is an unpublished work of Mentor Graphics Corporation.

TABLE OF CONTENTS

About This Manual iv

Getting Started with FPGA Advantage 1

Welcome to FPGA Advantage 1
Invoking FPGA Advantage 2
Exploring the Designs 4
Set the Default Language 5
Import the Fibonacci Design 6
Select Source HDL Files 6
Convert the Fibonacci Design 8
Browsing the Fibonacci Design 11
Examine the State Machine Text View 12
Generate HDL for the State Machine 13
Create Graphical Test Bench 15
Save the Test Bench 16
Simulate Your Design 17
Add Probes to the Test Bench 18
Add a Breakpoint 19
Run the Simulator 20
Complete the Simulation 21
Invoke LeonardoSpectrum 22
View the RTL Schematic 25
Further Information 26

Trademark Information

End-User License Agreement

About This Manual

This manual is a printable Acrobat PDF version of the online HTML *Getting Started with FPGA Advantage Tutorial*. It is provided for those users who prefer to work from a printed document.

The screen shots and path name convention (/) are the same as those used in the Windows environment. The screen shots shown in the Windows environment will look different to the ones that will appear when using the tutorial with UNIX workstations. However, the design flow is the same for any configuration on all platforms.

Getting Started with FPGA Advantage

Welcome to FPGA Advantage

This simple tutorial presents a complete design flow using a sample text design and Text HDL import, HDL generation, and simulation through to synthesis in approximately 30 minutes.

You should have installed at least one configuration of FPGA Advantage and obtained your evaluation or permanent licenses before starting this tutorial. Temporary evaluation licences can be obtained for *FPGA Advantage* or *FPGA Advantage Personal* from the FPGA Advantage website.

The design used in this Getting Started tutorial is based on HDL code recovered using HDL2Graphics technology. The tutorial can be completed for VHDL or Verilog using any of the *FPGA Advantage Pro* or *FPGA Advantage Personal Pro* configurations.

A number of HDL Designer Series tutorials can also be run. See the Start Here Guide for more information.

Invoking FPGA Advantage

You can invoke your installed configuration of FPGA Advantage on Windows by using the shortcut which was created by the install program on your desktop. Alternatively, you can choose the shortcut of your choice from the **FPGA Advantage 5.3** or **FPGA Advantage Personal 5.3** cascade of the **Programs** menu. One or more of the following options can be accessed from the Windows **Start** button if they are selected during installation.

FPGA Advantage for HDL Design

Shortcut	**Configuration**
FPGAdv Text	for FPGA Advantage Text
FPGAdv Graphics	for FPGA Advantage Graphics
FPGAdv Pro	for FPGA Advantage Pro

FPGA Advantage for Personal HDL Design

FPGAdv Personal Text	for FPGA Advantage Personal Text
FPGAdv Personal Graphics	for FPGA Advantage Personal Graphics
FPGAdv Personal Pro	for FPGA Advantage Personal Pro

FPGA Advantage for Personal Simulation

FPGAdv Personal Simulation Text	for FPGA Advantage Personal Simulation Text
FPGAdv Personal Simulation Graphics	for FPGA Advantage Personal Simulation Graphics
FPGAdv Personal Simulation Pro	for FPGA Advantage Personal Simulation Pro

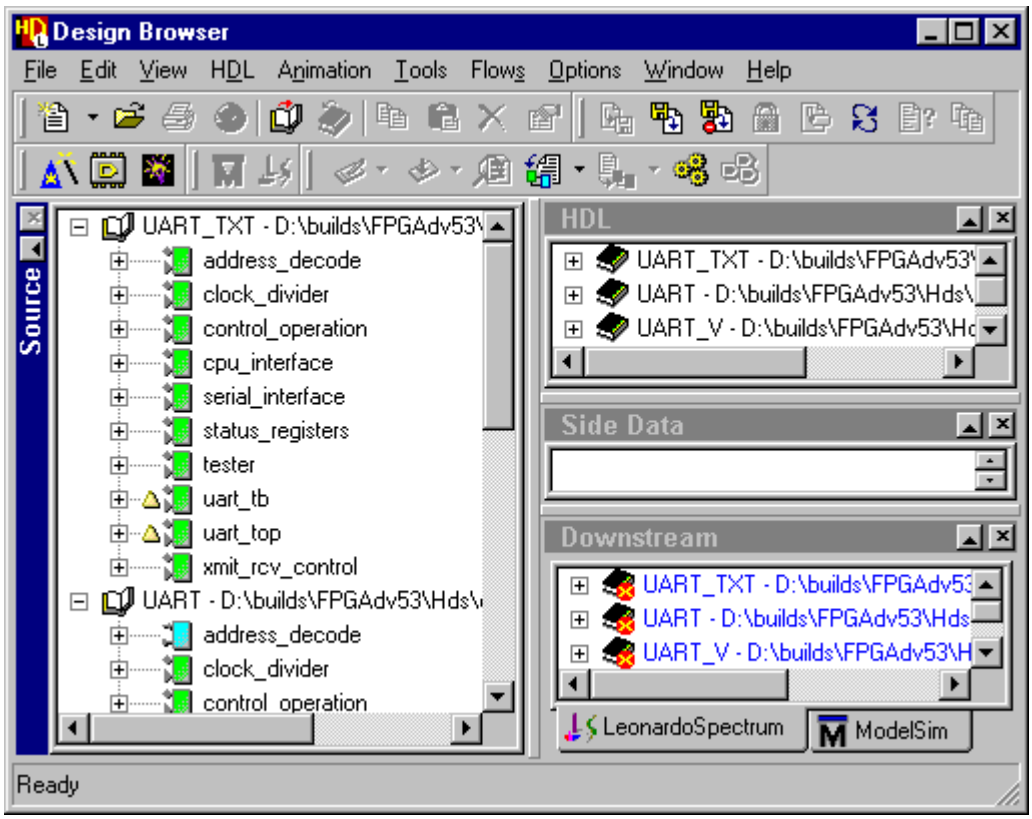
You can invoke FPGA Advantage on UNIX using one of the following scripts if they are selected during installation:

```
<install_path>/Fpgadv/bin/fpgadvtxt (FPGA Advantage Text)
<install_path>/Fpgadv/bin/fpgadvgfx (FPGA Advantage Graphics)
<install_path>/Fpgadv/bin/fpgadvpro (FPGA Advantage Pro)
```

Please refer to the FPGA Advantage Start Here Guide to see more information about the above configurations.

Exploring the Designs

The HDL Designer Series (HDS) design browser will be displayed when the tool is invoked:



The design browser window is divided into four browsers:

- **Source** shows the graphical and textual source design data.
- **HDL** shows the generated code.
- **Side Data** displays an expandable indented list showing design and user data associated with the design unit view selected in the source browser.
- **Downstream** is a tabbed window which shows the data files prepared for ModelSim and LeonardoSpectrum.

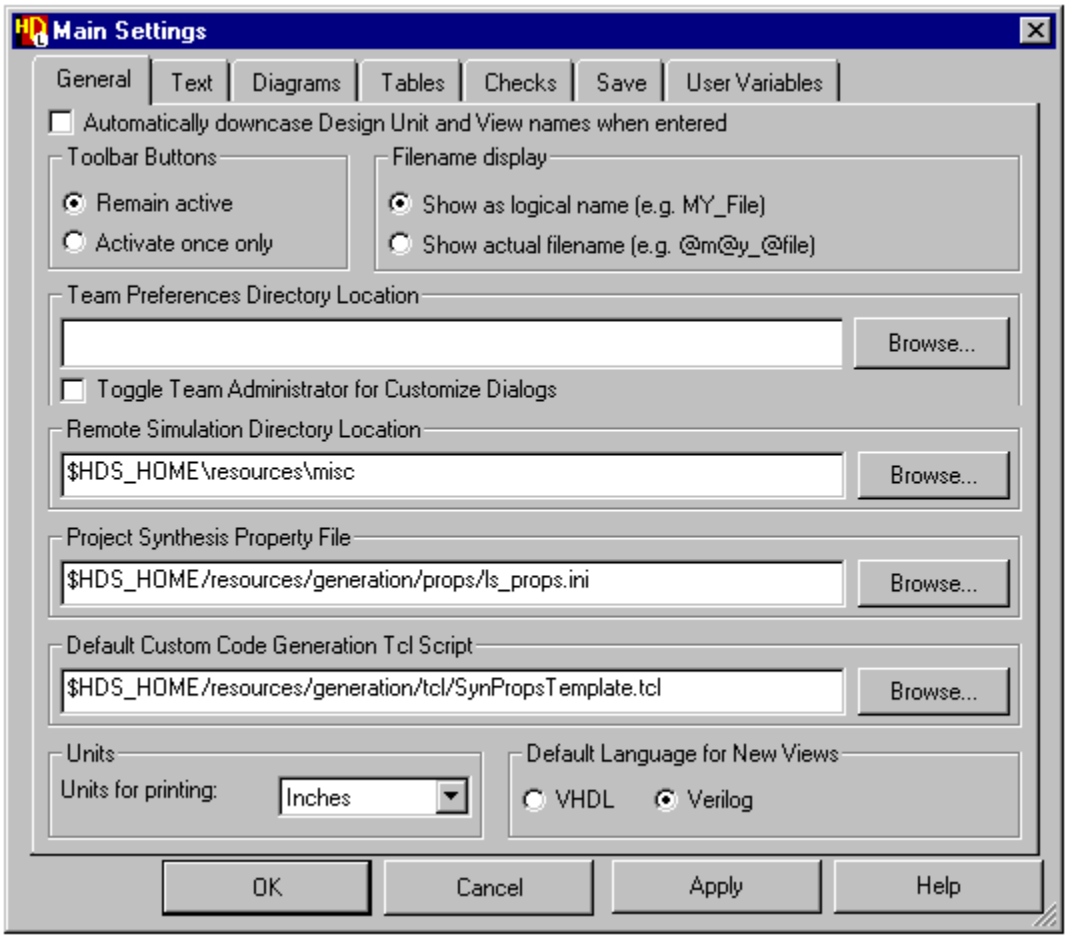
Three example libraries are displayed with their contents: a mixed language HDL text design named *UART_TXT*, a graphical VHDL design named *UART* and the corresponding graphical Verilog design named *UART_V*.

Set the Default Language

A set of default preferences are loaded when you invoke **FPGA Advantage** for the first time. There are separate tabbed dialog boxes for the main settings, VHDL and Verilog options, compile settings, HDL Import options, version management settings and master preferences for each type of graphical diagram. The preference dialog boxes can be accessed from the **Options** menu.

Choose **Main** from the **Options** menu to display the Main Settings dialog box. Select **Verilog** as the default language to be used for all new diagrams. Click the Apply and then the OK button to confirm your language choice.

(You can choose VHDL if you would like to run this tutorial using the VHDL language).



All other preferences can be left with their default values for this tutorial.

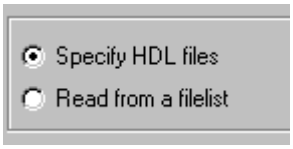
Import the Fibonacci Design

This tutorial uses a design which is supplied as VHDL or Verilog code and can be imported using the HDL Import Wizard. This will recover any VHDL or Verilog code using HDL Import technology and convert it into HDS text views. You can display the imported design using the existing design browser.

From the **File** menu choose **Close All Libraries**. All browsers in the design browser should now be empty.

Import the Fibonacci Design by choosing the pulldown on the button and select the option from the palette (or choose **Text HDL Import** from the **HDL Import** cascade of the **HDL** menu).

Select **Specify HDL files** in the first page of the HDL Import wizard:



This tutorial can be completed using either the VHDL or Verilog example code depending upon your language preference. The language will be determined automatically providing that the source code file extension is recognized in the general preferences.

Click the **Next** button to display the **Specify HDL Source Files** page of the **HDL Import** Wizard.

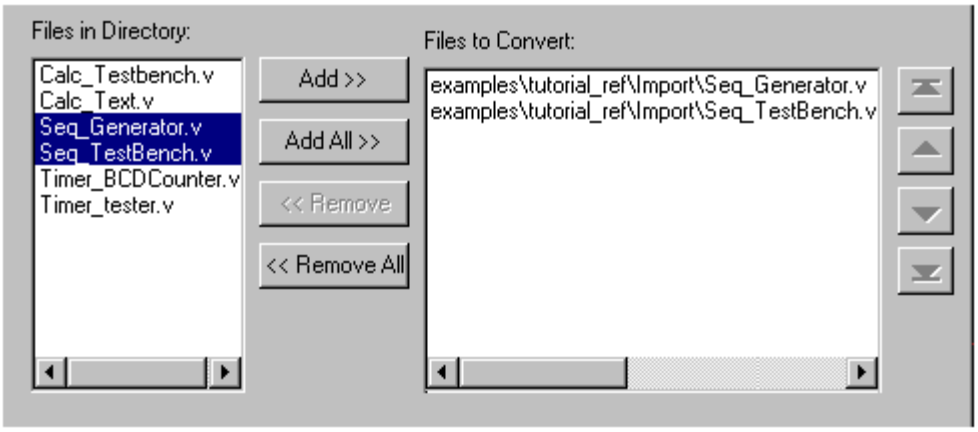
Select Source HDL Files

Use the **Browse** button to locate the Fibonacci sequencer source code in the examples sub-directory of your FPGA Advantage installation as shown in the entry box below. For example, if FPGA Advantage has been installed in the directory D:\Builds\FPGAdv53, the pathname to locate all source HDL files would be:

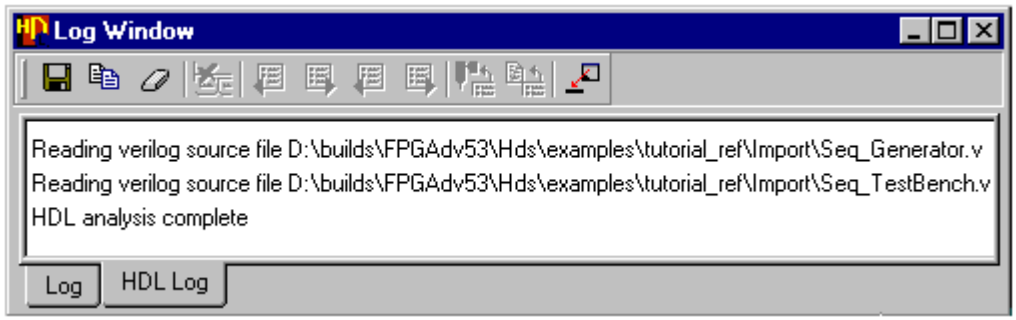
```
D:\Builds\FPGAdv53\Hds\examples\tutorial_ref\Import
```

Use the Files of type pulldown to select either VHDL or Verilog files. For example, Verilog files are shown selected below:

Select the *Seq_Generator* and the *Seq_TestBench* HDL files by using Ctrl + Left mouse button. Click Add >> to convert the files.

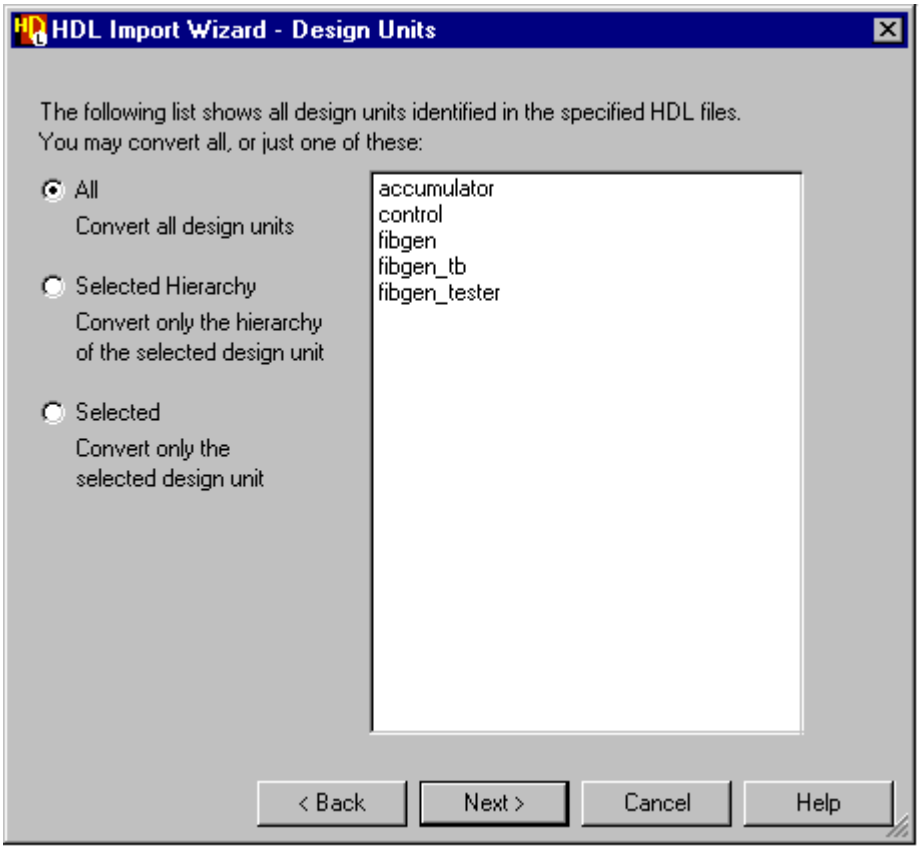


Click the **Next** button. You will now see the Log Window showing the Verilog source files for the Fibonacci design as they are read in:



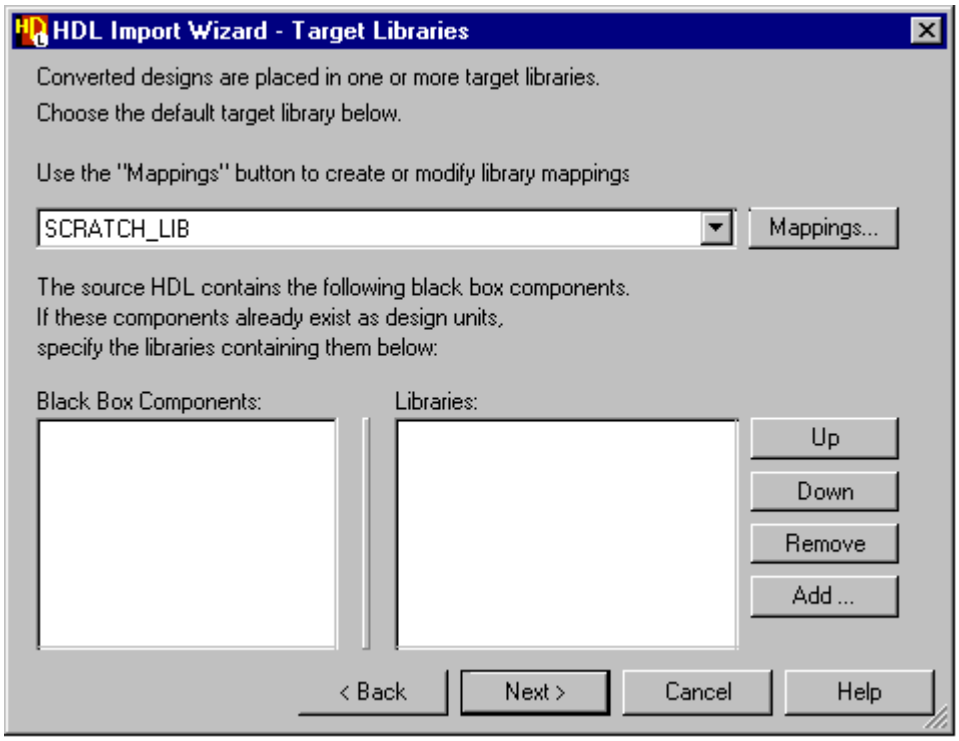
Convert the Fibonacci Design

Each design unit now appears in a separate window in the HDL Import Wizard ready for conversion.

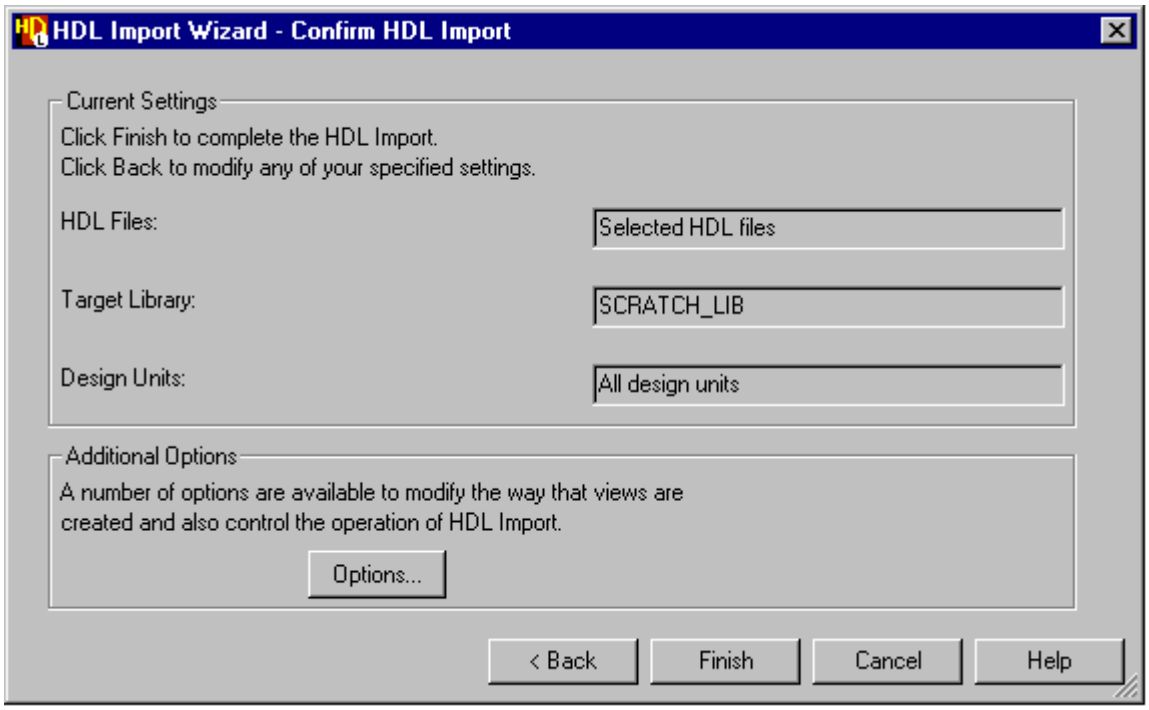


Click the **Next** button.

Select the SCRATCH_LIB library from the pulldown.


HDL Import Wizard - Target Libraries
Converted designs are placed in one or more target libraries.
Choose the default target library below.
Use the "Mappings" button to create or modify library mappings
SCRATCH_LIB
Mappings...
The source HDL contains the following black box components.
If these components already exist as design units,
specify the libraries containing them below:
Black Box Components:
Libraries:
Up
Down
Remove
Add ...
< Back
Next >
Cancel
Help

Click the **Next** button. The **Confirm HDL Import** dialog appears. Click the **Finish** button to convert the design.

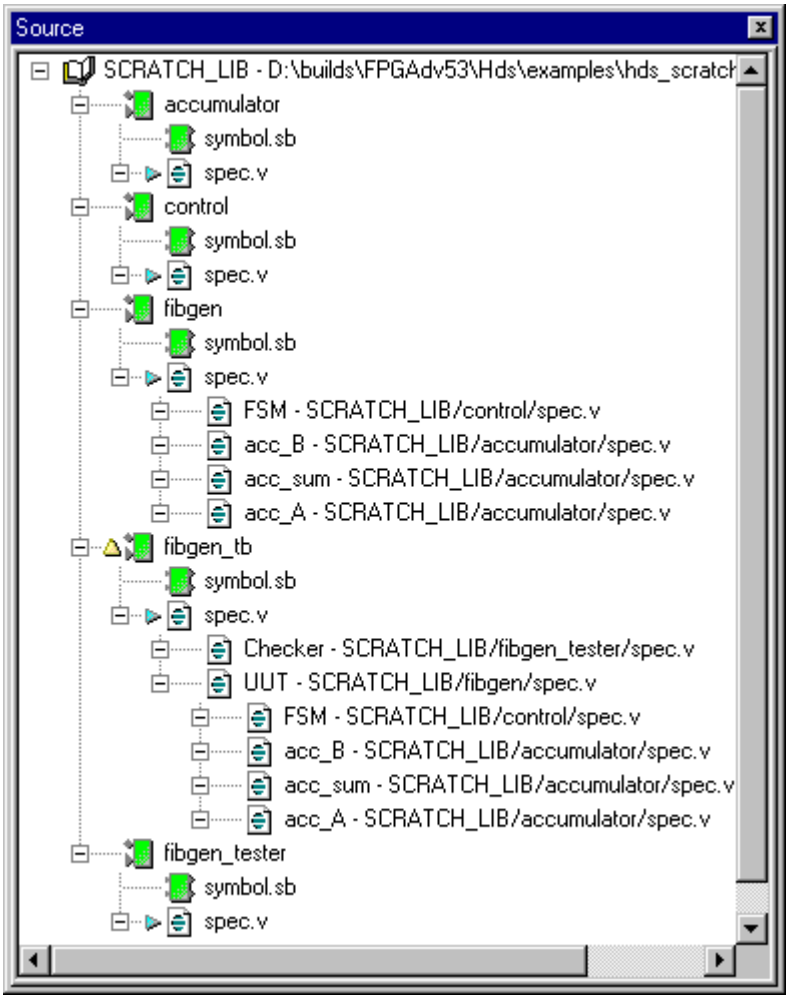


The HDL Log tab in the Log Window will indicate that a hierarchy of designs is being automatically created for the Fibonacci design and end with the following summary report:

```
5 HDS design units saved,
5 components
   5 HDL views
```

Browsing the Fibonacci Design

Select the SCRATCH_LIB library in the source browser. Click the right mouse button and choose **Expand All** from the popup menu. The design units for the Fibonacci design should now be displayed in the source browser as shown below:

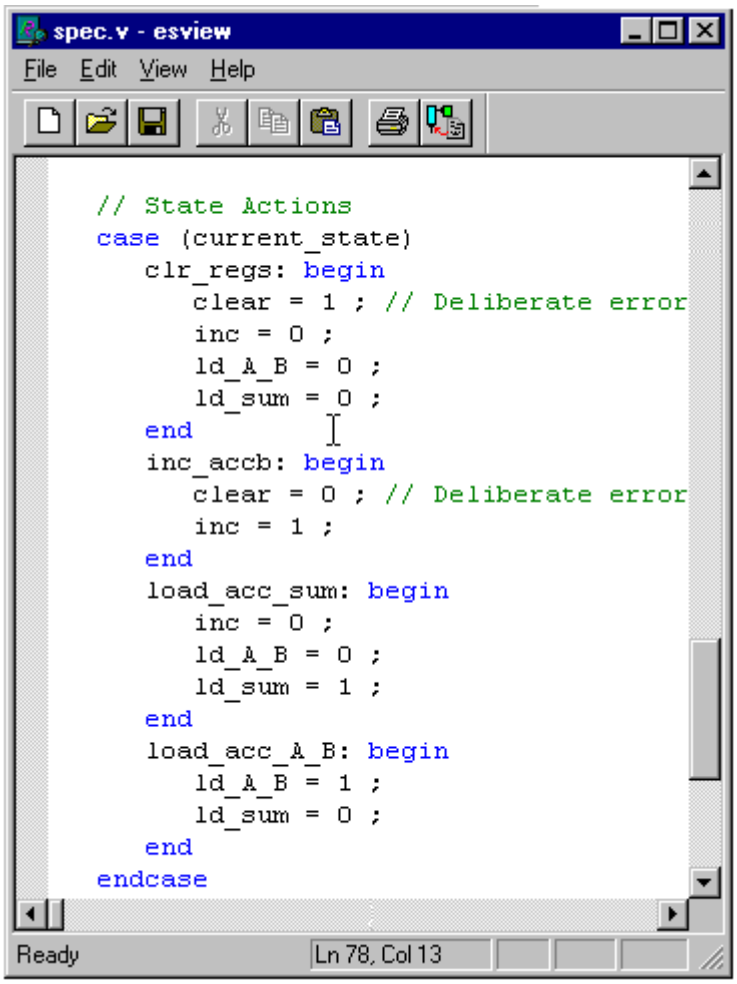


You can undock any of the 4 browsers from the design browser. This is achieved by holding down the left mouse button and dragging the window away from the browser. Alternatively, you can double-click the blue title bar to achieve the same result. Double-clicking a second time will return the window to the browser.

Examine the State Machine Text View

Double-click on the icon representing the *control* component design unit in the HDS design browser to display the following state machine in text view.

Use the scroll bar to view the code and notice that there are two deliberate errors which have been added.



The Verilog version of the state machine is shown. The VHDL version will be similar.

Close the text editor.

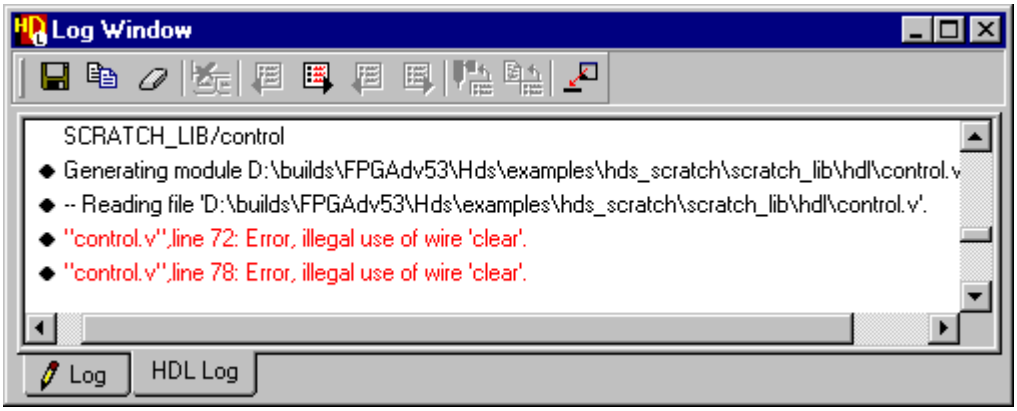
Generate HDL for the State Machine

Select the component design unit icon for *fibgen_tb* which is displayed with a "top of design" marker in the HDS design browser.

Generate HDL for the state machine by choosing the pulldown on the button and select the option from the palette (or choose **Hierarchy Through Components** from the **Generate** cascade of the **HDL** menu in the design browser).

Notice that the Log Window now displays two error messages which have been deliberately added to the state machine text view.

The signal *clear* has been incorrectly entered and needs replacing with *clr*.

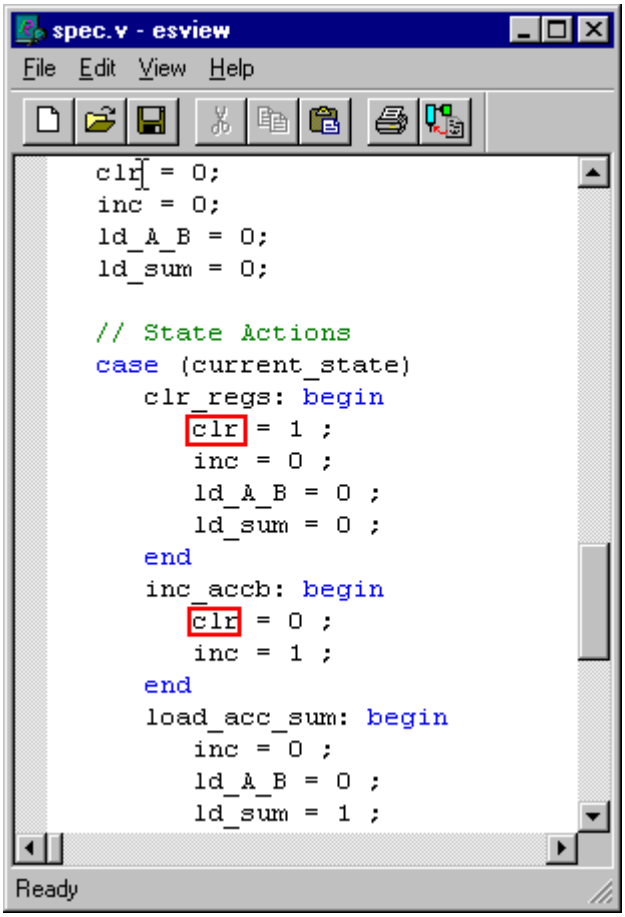


Correct the State Machine Errors

Make the Log Window active and double-click on the line containing the error in the log window. You should now be able to edit the code using the ESView text editor which appears by default.

Replace *clear* with the word *clr* and delete all of the comment text after the semi-colon. Save your changes and close the editor.

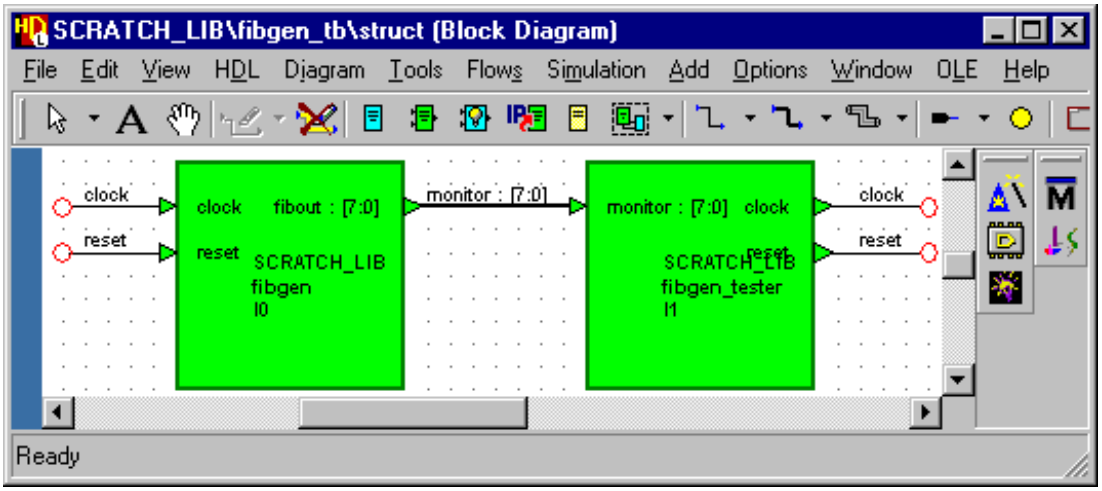
Repeat this procedure for the second occurrence of the error. The modified code should look similar to the example shown below.



Create Graphical Test Bench

Choose **Block Diagram** from the **New** cascade of the **File** menu in the design browser.

Use the button on the toolbar to display the Add Instance dialog box. Select the *SCRATCH_LIB* library and the *fibgen* component and click the OK button to add the *fibgen* component to the block diagram. Press the left mouse button and place the component on the diagram. Finally, press the right mouse button to clear the block outline (which is used to add multiple components). Repeat the same procedure and add the *fibgen_tester* component.



Position the mouse over the *fibgen* component and choose **Add Signal Stubs** from the popup menu. Two signals, *clock* and *reset* are added to the diagram plus a bus named *fibout.*

Repeat this procedure for the *fibgen_tester* component. The WARNING messages which appear can be ignored. This is because the net *clock* and *reset* already exist and the port and net declarations differ. Click OK to acknowledge the warning message.

Note from the diagram that two further *clock* and *reset* signals have been added plus a second bus named *monitor*.

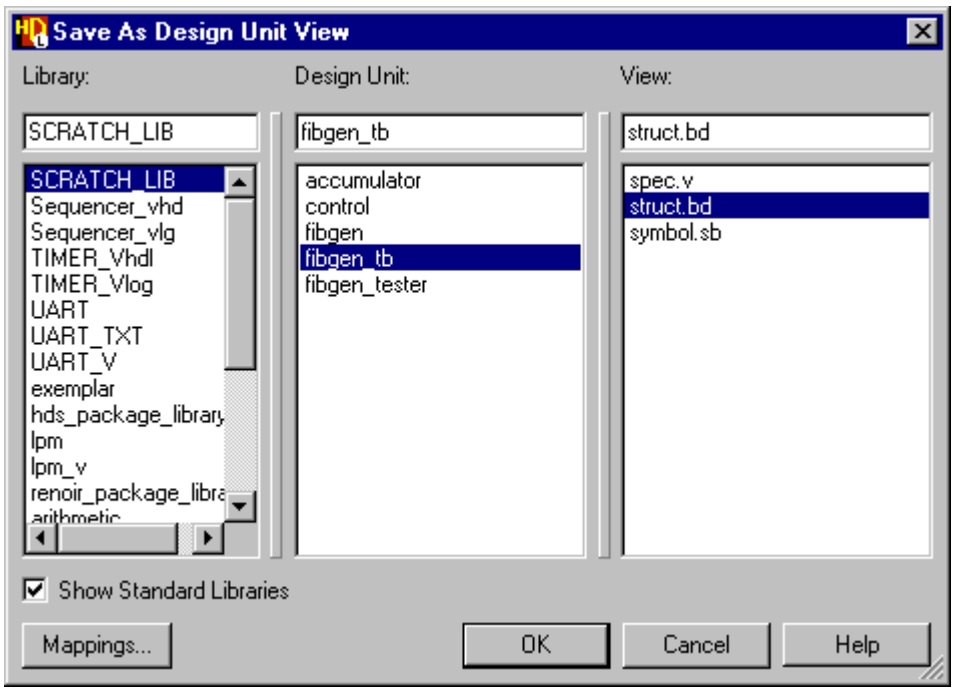
Select and delete the bus *fibout*. Drag and connect the bus *monitor* to the port *fibout.* The finished block diagram should look like the one shown on the previous page.

It is not necessary to explicitly connect the *clock* and *reset* signals between each port on the component and tester as these are implicitly connected by name.

Save the Test Bench

Use the button to save the test bench. The Save As Design Unit View dialog box is displayed which allows you to save a design unit into any currently mapped library. The columns allow you to specify the design unit name with its default view type.

Select the *SCRATCH-LIB* library and save the design unit name as *fibgen_tb*. The Save As dialog box should look similar to the example shown:



Click the button to save the test bench. Choose **Close Window** from the **File** menu and close the test bench block diagram.

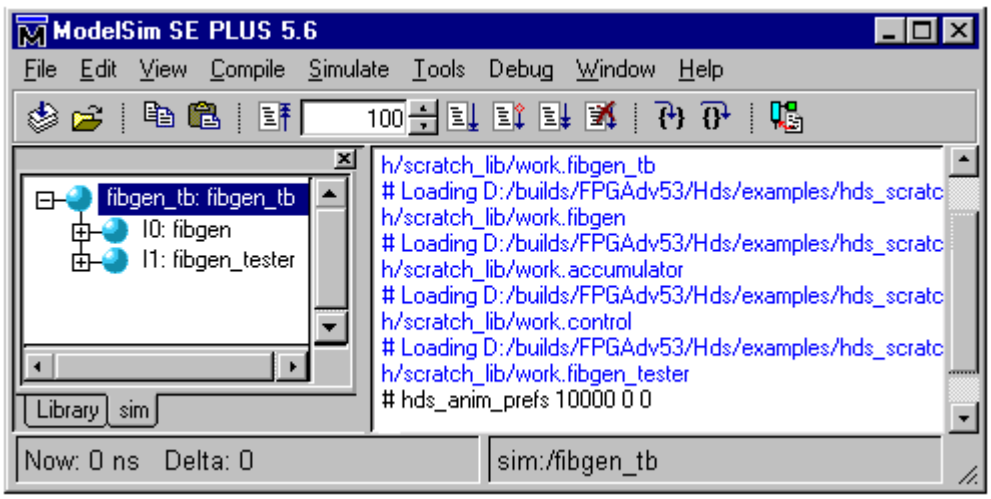
Simulate Your Design

Select *struct.bd* view below *fibgen_tb* from the design browser and choose **Set Default View** from the popup menu. This will define the graphical test bench view *struct.bd* as the default view before simulating the design. A blue triangle now appears next to *struct.bd* indicating that it is now the default view.

Select the *fibgen_tb* component and select the M button from the toolbar which will set up and automatically generate and compile HDL for the hierarchy below the selected design unit.The Start Model*Sim* dialog box will now appear.

Ensure that the **Enable Communications with HDS** option is set and click the OK button to confirm the dialog box.

If generation and compilation are completed successfully, the Model*Sim* simulator is invoked and the entire compiled design is loaded. Messages will now appear in the HDS Log Window confirming that the HDL has been compiled for all the HDS design units.

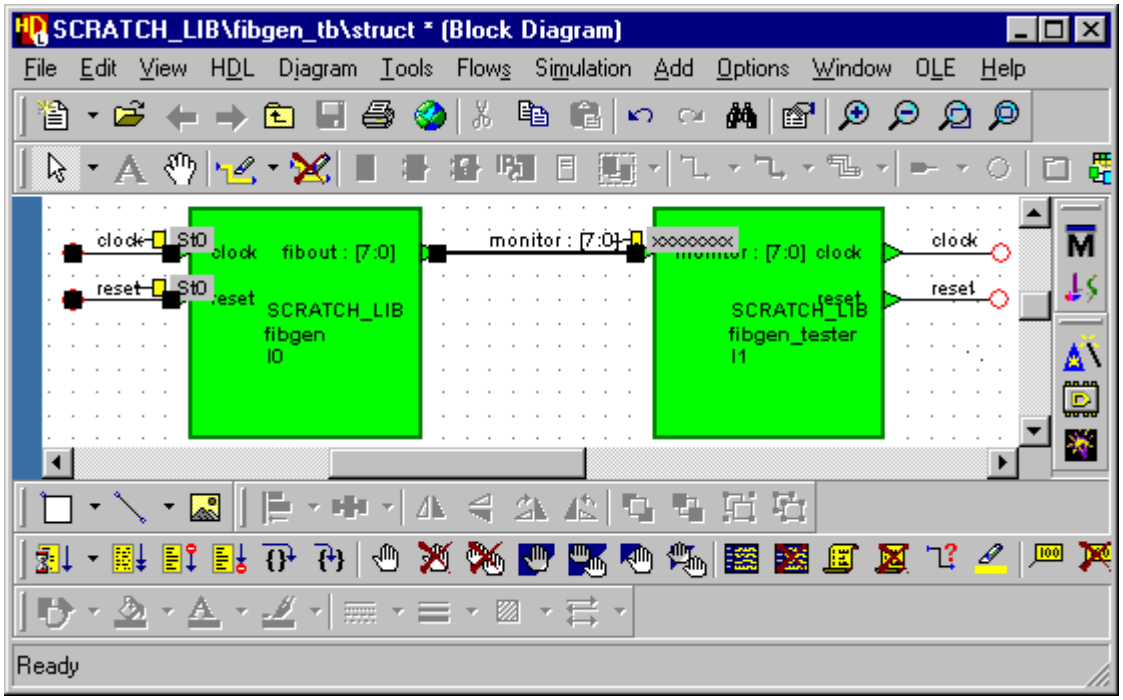


The progress of HDL generation and compilation are shown in the HDS Log Window. Notice that most design units are generated but all design units are compiled. If any compilation errors are detected when you compile a design, you can cross-reference from the HDS Log Window to the source graphics or generated HDL in the same way as for HDL generation errors.

Add Probes to the Test Bench

Open the *fibgen_tb* block diagram from the HDS design browser. Use the view area button or zoom in until the diagram looks similar to the one shown below. You can select multiple signals by using Shift + Left mouse button or by dragging a box crossing the required signals.

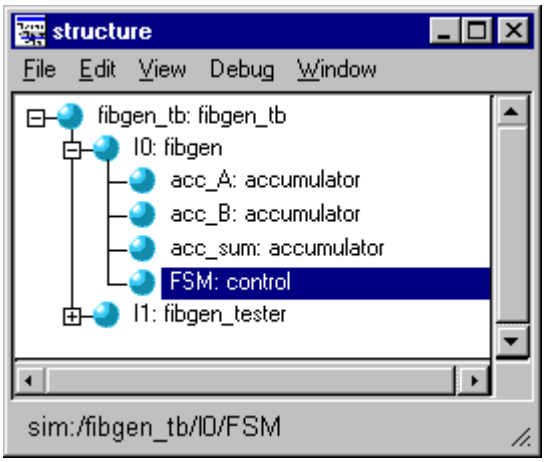
Select the two signals *clock* and *reset* and the bus *monitor* as shown in the diagram.



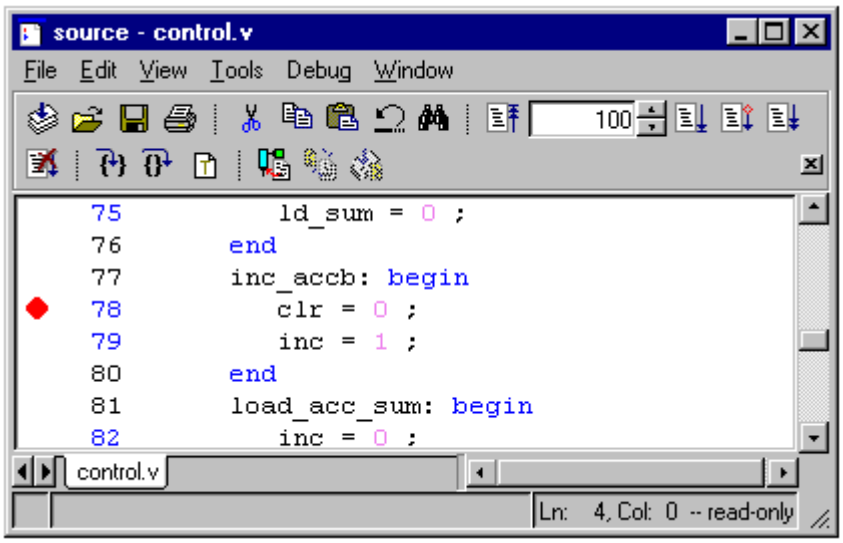
Notice that when the simulator is invoked there is an additional simulation toolbar displayed at the bottom of the HDS block diagram. Click the button to add simulation probes showing the current value of each signal.

Add a Breakpoint

In the *fibgen_tb* block diagram view, choose **Structure** from the **View** cascade of the **Simulation** menu in the design browser. A window showing the fibgen_tb hierarchy will appear. Expand the hierarchy underneath fibgen and select the *FSM: control* view.

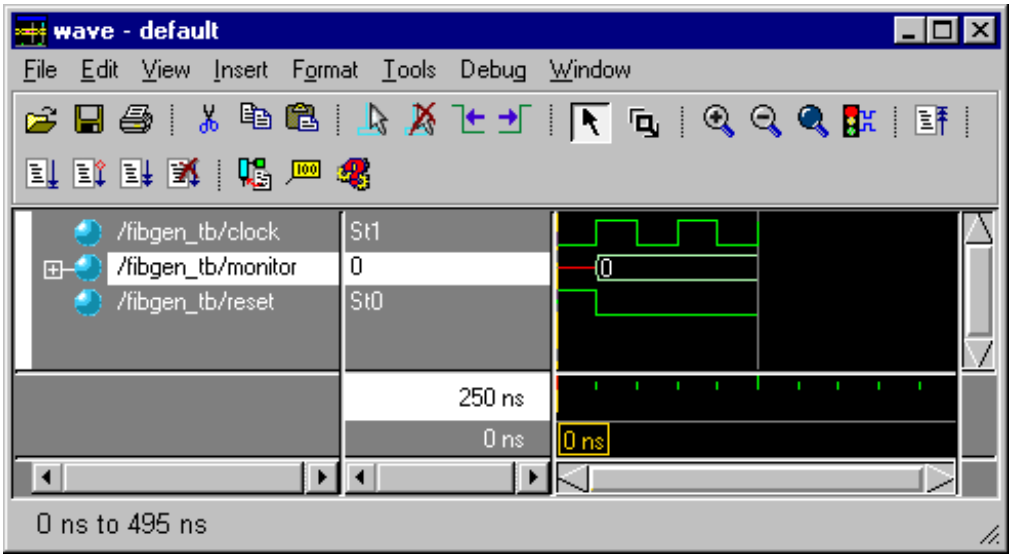


In the *fibgen_tb* block diagram view, choose **Source** from the **View** cascade of the **Simulation** menu. The state machine source window will appear as shown below. Navigate to line 78 and use the left mouse button to add a breakpoint to the line. Alternatively, choose the right mouse button and select **Enable Breakpoint 78** from the popup menu. A red dot will be shown indicating that a breakpoint is now set on line 78.



Run the Simulator

Make the *fibgen_tb* block diagram active and click the button to automatically open the ModelSim Wave window. Select the *fibgen_tb/monitor* bus as shown, and press the right mouse button and choose **Unsigned** for the **Radix** cascade of the popup menu.



In the *fibgen_tb* block diagram view click the to advance simulation by the default simulator timestep (100 nanoseconds). Notice that the signal values are initialized in the simulation probes on the test bench block diagram.

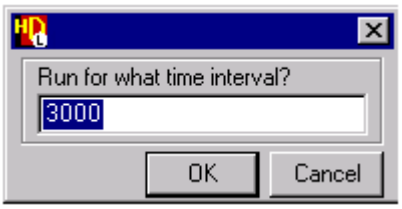
Click the button to run the simulator until the next breakpoint. Notice that the waveform appears as the simulation advances. Notice that an arrow appears over the red dot in the *control.v* source window.

Finally, make sure that the *control.v* source window is active and remove the remaining breakpoint by choosing **Remove Breakpoint 78** from the popup menu.

Alternatively, choose **Breakpoints** from the **Tools** menu. A dialog box will appear showing all breakpoints currently set. Select the breakpoint which appears on line 78 and press the **Delete** button. Click **OK** to close the dialog box.

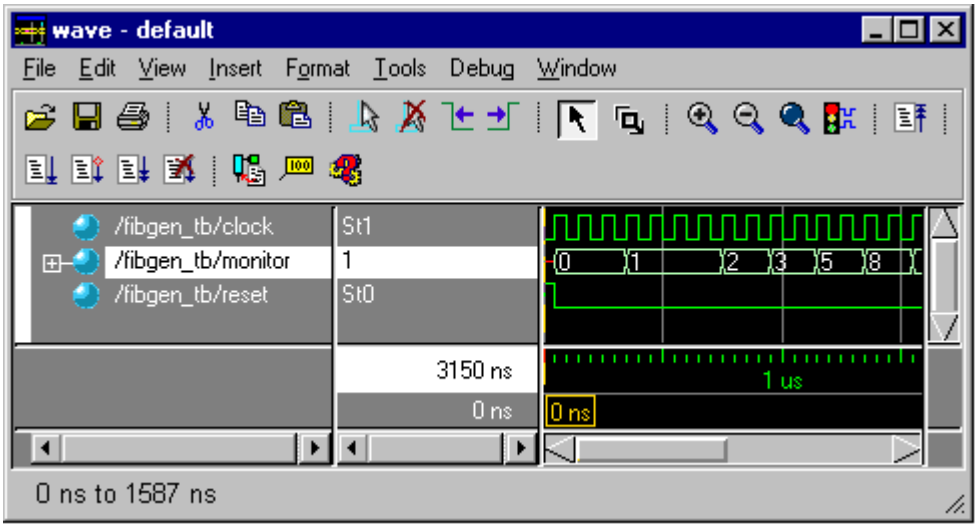
Complete the Simulation

In the fibgen block diagram click the button adjacent to the button on the toolbar and select **Choose** from the popup menu. Another dialog will appear prompting you to enter a time interval to run the simulator. Enter 3000 into the entry box and click **OK** to run the simulator.



Alternatively, you can enter a time interval in the ModelSim window and then run the simulator.

Make the Model*Sim* Wave window active and choose **Zoom Full** from the **Zoom** cascade of the **View** menu. This will display the full simulation waveforms which should look similar to the picture below for a successfully verified design.



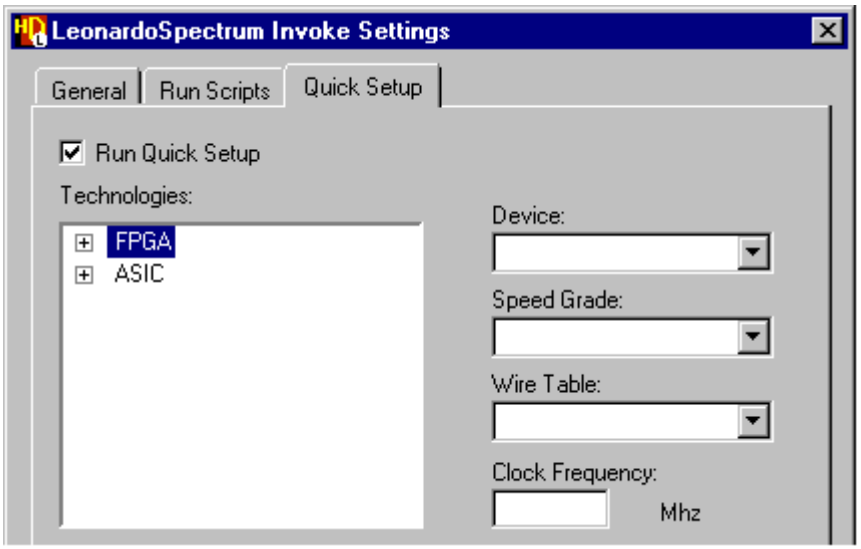
Simulation is now complete. Choose **Quit** from the ModelSim **File** menu to exit from the simulator. Click **Yes** to the exit message and close the HDS block diagram.

Invoke LeonardoSpectrum

Select the *fibgen* component in the HDS design browser and then click on the button. The LeonardoSpectrum Invoke Settings dialog is displayed.

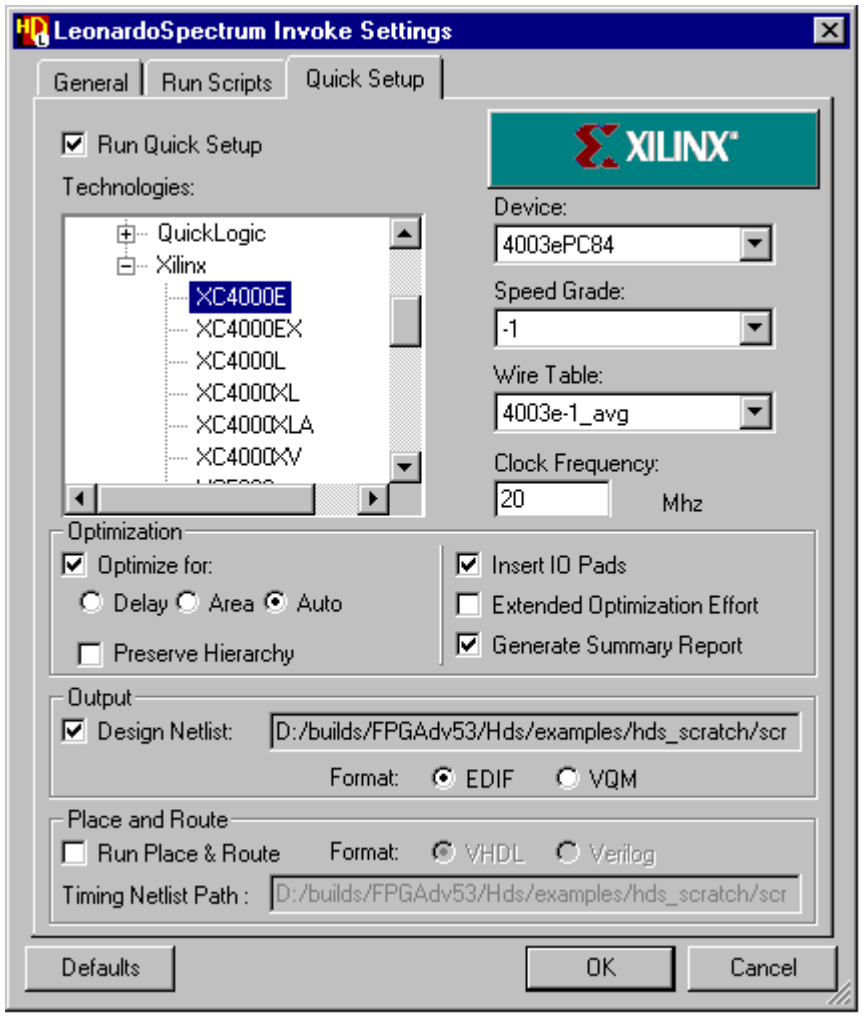
You cannot synthesize a test bench, so you must select the top level design unit for the actual design you want to synthesize.

Select the technology of your choice in the **Quick Setup** tab. For example, choose FPGA and Xilinx XC4000E by using the ⊞ buttons to expand the list of FPGA technologies available.



If you are using the *FPGA Advantage Personal* configuration with level 2 synthesis, ASIC libraries are not available and you can choose the Xilinx library directly.

When you select a technology, default values are automatically entered in the **Device, Speed Grade,** and **Wire Table** fields (these may vary from the ones shown below). The remaining fields will be set by default. Enter the value **20** in the **Clock Frequency** field and synthesize your design by clicking the **OK** button.

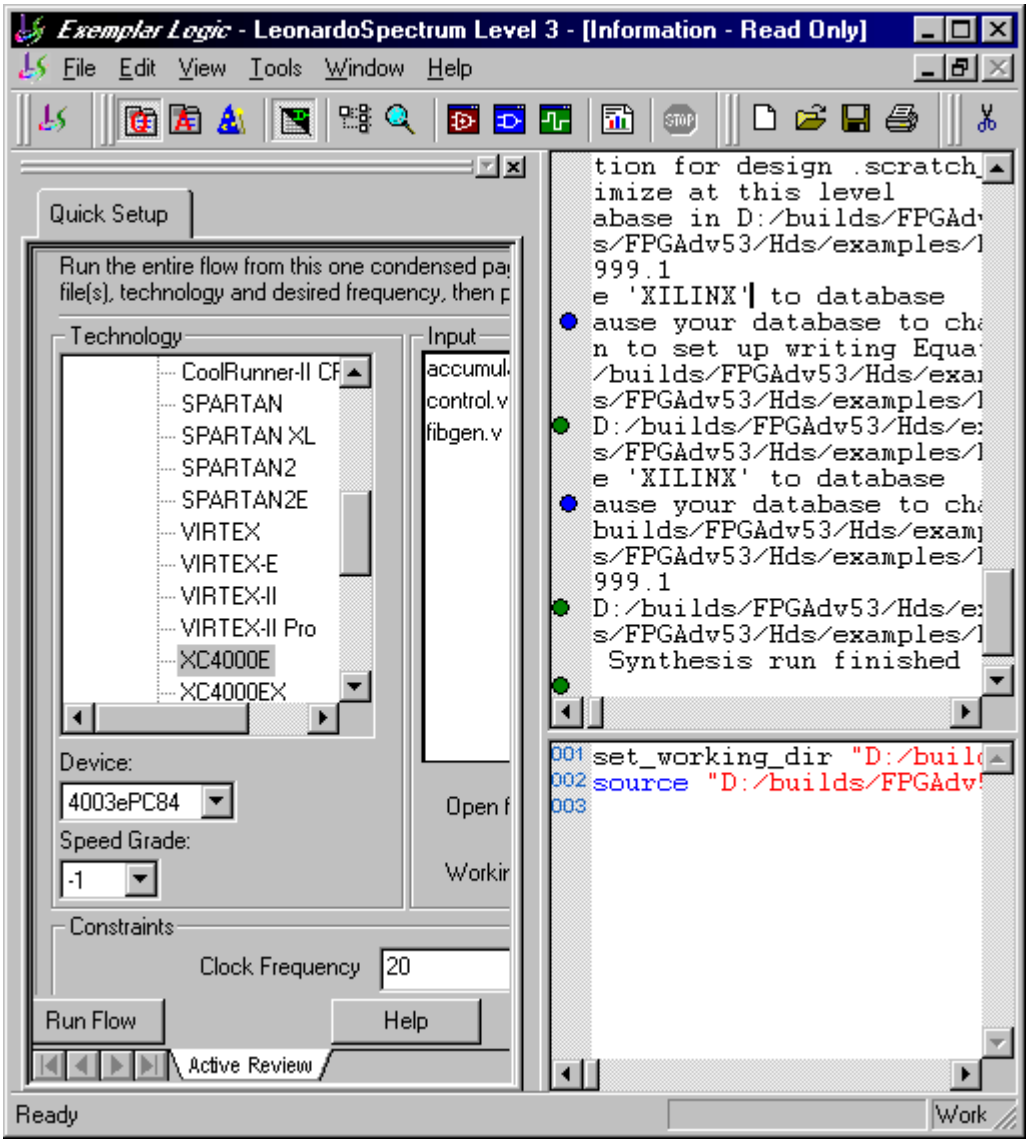


You are prompted to confirm the LeonardoSpectrum license.

You must choose a Level 2 license if you are using any of the *FPGA Advantage Personal* configurations. If you are using any of the *FPGA Advantage* configurations, select a Level 3 license. You can uncheck the **Run license selection next time** option if you want to run synthesis without prompting for the license level next time you invoke.

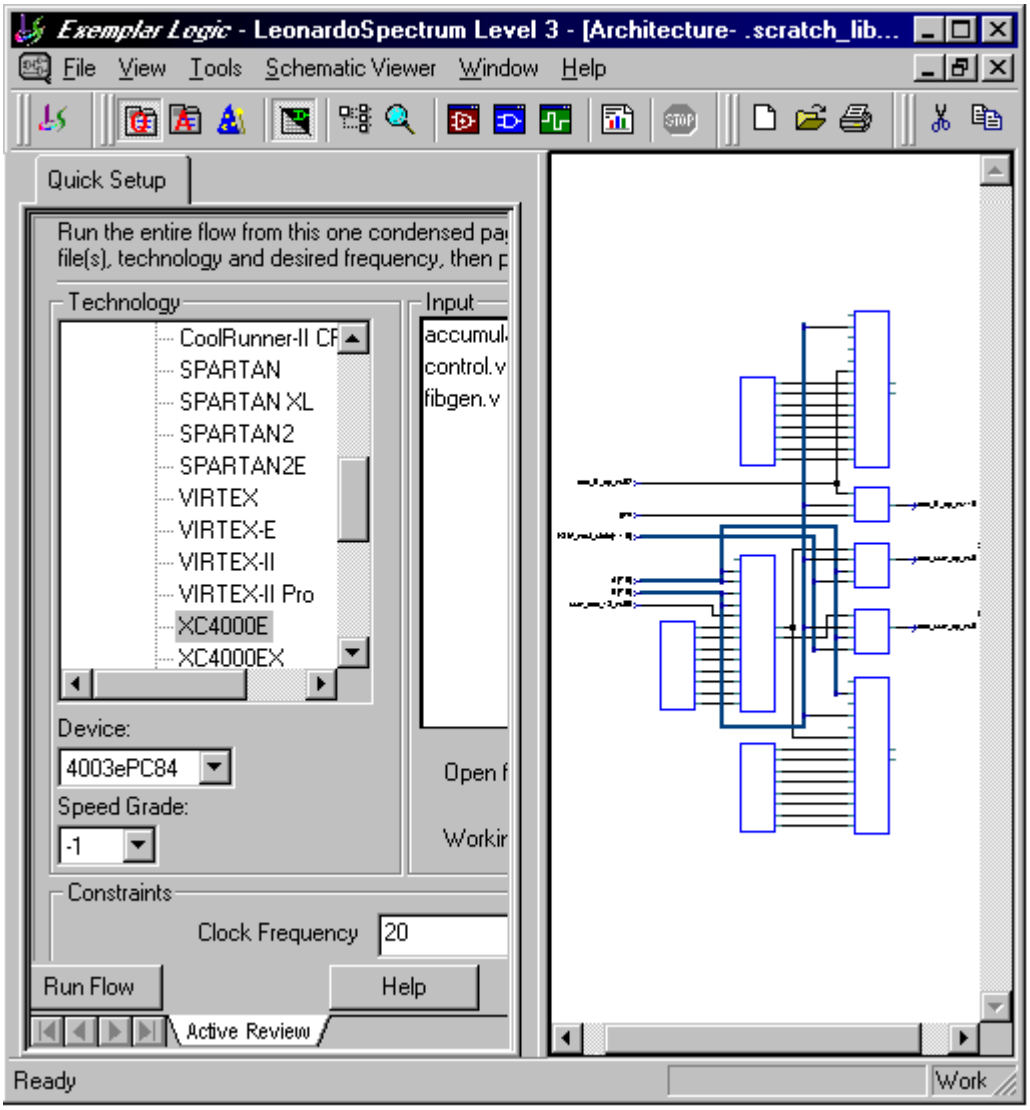
A Tip of the Day dialog box may appear. Click **OK** to clear the dialog box and LeonardoSpectrum is invoked on the entire design and the HDL files for your design are shown in the **Quick Setup** tab.

LeonardoSpectrum will optimize the design. Progress and completion messages will be displayed in the information window showing that the synthesis run has finished.



View the RTL Schematic

If you are using the Level 3 license for LeonardoSpectrum, you can display an RTL Schematic for your design by clicking the button. You can move around the schematic using the scroll bars and the diagram can be enlarged inside the browser by choosing **Zoom In** from the **Zoom** cascade of the **Schematic Viewer** pulldown menu.



The Schematic Viewer is not available with a LeonardoSpectrum level 2 license. However, a license can be added if you obtain an additional license feature for LeonardoInsight.

You can cross-probe from the schematic to the corresponding object in a HDS source diagram. This is achieved by selecting an instance on the schematic and clicking the right mouse button. To view the HDS source diagram choose **Trace to HDL Designer** from the popup menu. The relevant HDS design unit view is displayed.

Close the text editor windows and do the following:

Exit from LeonardoSpectrum by choosing **Exit** from the LeonardoSpectrum **File** menu, choosing **No** from the confirmation dialog box.

Exit from HDS by choosing **Exit** from the **File** menu in the Design Browser window and choosing **Yes** from the confirmation dialog box.

Further Information

You have now completed the FPGA Advantage *Getting Started Tutorial* and seen the complete design flow from importing HDL into HDS, through verification using the ModelSim simulator and used LeonardoSpectrum to synthesize a gate level netlist.

Each of these tools support a large range of features which cannot be illustrated in this simple tutorial. For more information, see the documentation which is available from the **Help** menu in each tool.

You can also access documentation from the **FPGA Advantage 5.3 > Bookcase** which can be opened on Windows from the **Programs** cascade of the **Start** menu. On UNIX, this document can be accessed by opening the Adobe Acrobat document *DocIndex.pdf* which can be found in the FPGA Advantage installation at: `<install_dir>/Doc/DocIndex.pdf.`

The **FPGA Advantage Bookcase** can also be accessed from the **Help** pulldown menu in the design browser on both Windows and UNIX by selecting **Help > FPGA Advantage Bookcase.**

Trademark Information

The following names which appear in this documentation set are trademarks, registered trademarks or service marks of Mentor Graphics Corporation:

HDL Designer Series™, HDL Designer™, HDL Pilot™, HDL Detective™, HDL Author™, HDL2Graphics™, FPGA Advantage™, Interconnect Table™, Interface-Based Design™, IBD™, Inventra™, LeonardoInsight™, LeonardoSpectrum™, Mentor™, Mentor Graphics®, Model*Sim*®, ModuleWare™, Renoir™, Seamless®, Seamless CVE™ and SpeedGate™.

The following names which appear in this documentation set are trademarks, registered trademarks or service marks of other companies:

Adobe, the Adobe logo, Acrobat, the Acrobat logo, Exchange, FrameMaker and PostScript are registered trademarks of Adobe Systems Incorporated.

Altera, APEX, MegaWizard and MAX+PLUS are registered trademarks and Quartus a trademark of Altera Corporation.

ClearCase Attache is a trademark and ClearCase is a registered trademark of Rational Software Corporation.

DesignSync is a registered trademark of Synchronicity Incorporated.

FLEXlm is a trademark of Globetrotter Software, Incorporated.

Hewlett-Packard (HP), HP-UX and PA-RISC are registered trademarks of Hewlett-Packard Company.

Leapfrog, NC-Verilog, Verilog and Verilog-XL are trademarks and registered trademarks of Cadence Design Systems Incorporated.

Netscape is a trademark of Netscape Communications Corporation.

SPARC is a registered trademark and SPARCstation is a trademark of SPARC International Incorporated.

SpyGlass is a trademark of Interra Inc.

Sun Microsystems and Sun Workstation are registered trademarks of Sun Microsystems Incorporated. Sun and SunOS are trademarks of Sun Microsystems Incorporated.

Synopsys, Design Analyzer, Design Compiler, FPGA Express, VCS, VCSi and VSS are trademarks of Synopsys Incorporated.

Synplify is a registered trademark of Synplicity Incorporated.

The Graphics Connection is a trademark of Square One.

Visual SourceSafe and Windows are trademarks of Microsoft Corporation.

UNIX is a registered trademark of UNIX System Laboratories, Incorporated.

Xilinx is a registered trademark and Core Generator a trademark of Xilinx, Incorporated.

Other brand or product names that appear in the documentation are trademarks or registered trademarks of their respective holders.

End-User License Agreement

IMPORTANT - USE OF THIS SOFTWARE IS SUBJECT TO LICENSE RESTRICTIONS CAREFULLY READ THIS LICENSE AGREEMENT BEFORE USING THE SOFTWARE

This license is a legal "Agreement" concerning the use of Software between you, the end-user, either individually or as an authorized representative of the company purchasing the license, and Mentor Graphics Corporation, Mentor Graphics (Ireland) Limited, Mentor Graphics (Singapore) Private Limited, and their majority-owned subsidiaries ("Mentor Graphics"). USE OF SOFTWARE INDICATES YOUR COMPLETE AND UNCONDITIONAL ACCEPTANCE OF THE TERMS AND CONDITIONS SET FORTH IN THIS AGREEMENT. If you do not agree to these terms and conditions, promptly return or, if received electronically, certify destruction of Software and all accompanying items within 10 days after receipt of Software and receive a full refund of any license fee paid

END-USER LICENSE AGREEMENT

1. **GRANT OF LICENSE**. The software programs you are installing, downloading, or have acquired with this Agreement, including any updates, modifications, revisions, copies, and documentation ("Software") are copyrighted, trade secret and confidential information of Mentor Graphics or its licensors who maintain exclusive title to all Software and retain all rights not expressly granted by this Agreement. Mentor Graphics or its authorized distributor grants to you, subject to payment of appropriate license fees, a nontransferable, nonexclusive license to use Software solely: (a) (in machine-readable, object-code form; (b) for your internal business purposes; and (c) on the computer hardware or at the site for which an applicable license fee is paid, or as authorized by Mentor Graphics. A site is restricted to a one-half mile (800 meter) radius. Mentor Graphics' then-current standard policies, which vary depending on Software, license fees paid or service plan purchased, apply to the following and are subject to change: (a) relocation of Software; (b) use of Software, which may be limited, for example, to execution of a single session by a single user on the authorized hardware or for a restricted period of time (such limitations may be communicated and technically implemented through the use of authorization codes or similar devices); (c) eligibility to receive updates, modifications, and revisions; and (d) support services provided. Current standard policies are available upon request.

2. **ESD SOFTWARE**. If you purchased a license to use embedded software development (ESD) Software, Mentor Graphics or its authorized distributor grants to you a nontransferable, nonexclusive license to reproduce and distribute executable files created using ESD compilers, including the ESD run-time libraries distributed with ESD C and C++ compiler Software that are linked into a composite program as an integral part of your compiled computer program, provided that you distribute these files only in conjunction with your compiled computer program. Mentor Graphics does NOT grant you any right to duplicate or incorporate copies of Mentor Graphics' real-time operating systems or other ESD Software, except those explicitly granted in this section, into your products without first signing a separate agreement with Mentor Graphics for such purpose.

3. **BETA CODE**

   3.1. Portions or all of certain Software may contain code for experimental testing and evaluation ("Beta Code"), which may not be used without Mentor Graphics' explicit authorization. Upon Mentor Graphics' authorization, Mentor Graphics grants to you a temporary, nontransferable, nonexclusive license for experimental use to test and evaluate the Beta Code without charge for a limited period of time specified by Mentor Graphics. This grant and your use of the Beta Code shall not be construed as marketing or offering to sell a license to the Beta Code, which Mentor Graphics may choose not to release commercially in any form.

3.2. If Mentor Graphics authorizes you to use the Beta Code, you agree to evaluate and test the Beta Code under normal conditions as directed by Mentor Graphics. You will contact Mentor Graphics periodically during your use of the Beta Code to discuss any malfunctions or suggested improvements. Upon completion of your evaluation and testing, you will send to Mentor Graphics a written evaluation of the Beta Code, including its strengths, weaknesses and recommended improvements.

3.3. You agree that any written evaluations and all inventions, product improvements, modifications or developments that Mentor Graphics conceives or makes during or subsequent to this Agreement, including those based partly or wholly on your feedback, will be the exclusive property of Mentor Graphics. Mentor Graphics will have exclusive rights, title and interest in all such property. The provisions of this subsection shall survive termination or expiration of this Agreement.

4. **RESTRICTIONS ON USE**. You may copy Software only as reasonably necessary to support the authorized use. Each copy must include all notices and legends embedded in Software and affixed to its medium and container as received from Mentor Graphics. All copies shall remain the property of Mentor Graphics or its licensors. You shall maintain a record of the number and primary location of all copies of Software, including copies merged with other software, and shall make those records available to Mentor Graphics upon request. You shall not make Software available in any form to any person other than your employer's employees and contractors, excluding Mentor Graphics' competitors, whose job performance requires access. You shall take appropriate action to protect the confidentiality of Software and ensure that any person permitted access to Software does not disclose it or use it except as permitted by this Agreement. Except as otherwise permitted for purposes of interoperability as specified by the European Union Software Directive or local law, you shall not reverse-assemble, reverse-compile, reverse-engineer or in any way derive from Software any source code. You may not sublicense, assign or otherwise transfer Software, this Agreement or the rights under it without Mentor Graphics' prior written consent. The provisions of this section shall survive the termination or expiration of this Agreement.

5. **LIMITED WARRANTY**

5.1. Mentor Graphics warrants that during the warranty period Software, when properly installed, will substantially conform to the functional specifications set forth in the applicable user manual. Mentor Graphics does not warrant that Software will meet your requirements or that operation of Software will be uninterrupted or error free. The warranty period is 90 days starting on the 15th day after delivery or upon installation, whichever first occurs. You must notify Mentor Graphics in writing of any nonconformity within the warranty period. This warranty shall not be valid if Software has been subject to misuse, unauthorized modification or installation. MENTOR GRAPHICS' ENTIRE LIABILITY AND YOUR EXCLUSIVE REMEDY SHALL BE, AT MENTOR GRAPHICS' OPTION, EITHER (A) REFUND OF THE PRICE PAID UPON RETURN OF SOFTWARE TO MENTOR GRAPHICS OR (B) MODIFICATION OR REPLACEMENT OF SOFTWARE THAT DOES NOT MEET THIS LIMITED WARRANTY, PROVIDED YOU HAVE OTHERWISE COMPLIED WITH THIS AGREEMENT. MENTOR GRAPHICS MAKES NO WARRANTIES WITH RESPECT TO: (A) SERVICES; (B) SOFTWARE WHICH IS LOANED TO YOU FOR A LIMITED TERM OR AT NO COST; OR (C) EXPERIMENTAL BETA CODE; ALL OF WHICH ARE PROVIDED "AS IS."

5.2. THE WARRANTIES SET FORTH IN THIS SECTION 5 ARE EXCLUSIVE. NEITHER MENTOR GRAPHICS NOR ITS LICENSORS MAKE ANY OTHER WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO SOFTWARE OR OTHER MATERIAL PROVIDED UNDER THIS AGREEMENT. MENTOR GRAPHICS AND ITS LICENSORS SPECIFICALLY DISCLAIM ALL IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

6. **LIMITATION OF LIABILITY**. EXCEPT WHERE THIS EXCLUSION OR RESTRICTION OF LIABILITY WOULD BE VOID OR INEFFECTIVE UNDER APPLICABLE STATUTE OR REGULATION, IN NO EVENT SHALL MENTOR GRAPHICS OR ITS LICENSORS BE LIABLE FOR INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES (INCLUDING LOST PROFITS OR SAVINGS) WHETHER BASED ON CONTRACT, TORT OR ANY OTHER LEGAL THEORY, EVEN IF MENTOR GRAPHICS OR ITS LICENSORS HAVE BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. IN NO EVENT SHALL MENTOR GRAPHICS' OR ITS LICENSORS' LIABILITY UNDER THIS AGREEMENT EXCEED THE AMOUNT PAID BY YOU FOR THE SOFTWARE OR SERVICE GIVING RISE TO THE CLAIM. IN THE CASE WHERE NO AMOUNT WAS PAID, MENTOR GRAPHICS AND ITS LICENSORS SHALL HAVE NO LIABILITY FOR ANY DAMAGES WHATSOEVER.

7. **LIFE ENDANGERING ACTIVITIES**. NEITHER MENTOR GRAPHICS NOR ITS LICENSORS SHALL BE LIABLE FOR ANY DAMAGES RESULTING FROM OR IN CONNECTION WITH THE USE OF SOFTWARE IN ANY APPLICATION WHERE THE FAILURE OR INACCURACY OF THE SOFTWARE MIGHT RESULT IN DEATH OR PERSONAL INJURY. YOU AGREE TO INDEMNIFY AND HOLD HARMLESS MENTOR GRAPHICS AND ITS LICENSORS FROM ANY CLAIMS, LOSS, COST, DAMAGE, EXPENSE, OR LIABILITY, INCLUDING ATTORNEYS' FEES, ARISING OUT OF OR IN CONNECTION WITH SUCH USE.

8. **INFRINGEMENT**

   8.1. Mentor Graphics will defend or settle, at its option and expense, any action brought against you alleging that Software infringes a patent or copyright in the United States, Canada, Japan, Switzerland, Norway, Israel, Egypt, or the European Union. Mentor Graphics will pay any costs and damages finally awarded against you that are attributable to the claim, provided that you: (a) notify Mentor Graphics promptly in writing of the action; (b) provide Mentor Graphics all reasonable information and assistance to settle or defend the claim; and (c) grant Mentor Graphics sole authority and control of the defense or settlement of the claim.

   8.2. If an infringement claim is made, Mentor Graphics may, at its option and expense, either (a) replace or modify Software so that it becomes noninfringing, or (b) procure for you the right to continue using Software. If Mentor Graphics determines that neither of those alternatives is financially practical or otherwise reasonably available, Mentor Graphics may require the return of Software and refund to you any license fee paid, less a reasonable allowance for use.

   8.3. Mentor Graphics has no liability to you if the alleged infringement is based upon: (a) the combination of Software with any product not furnished by Mentor Graphics; (b) the modification of Software other than by Mentor Graphics; (c) the use of other than a current unaltered release of Software; (d) the use of Software as part of an infringing process; (e) a product that you design or market; (f) any Beta Code contained in Software; or (g) any Software provided by Mentor Graphics' licensors which do not provide such indemnification to Mentor Graphics' customers.

   8.4. THIS SECTION 8 STATES THE ENTIRE LIABILITY OF MENTOR GRAPHICS AND ITS LICENSORS AND YOUR SOLE AND EXCLUSIVE REMEDY WITH RESPECT TO ANY ALLEGED PATENT OR COPYRIGHT INFRINGEMENT BY ANY SOFTWARE LICENSED UNDER THIS AGREEMENT.

9. **TERM**. This Agreement remains effective until expiration or termination. This Agreement will automatically terminate if you fail to comply with any term or condition of this Agreement or if you fail to pay for the license when due and such failure to pay continues for a period of 30 days after written notice from Mentor Graphics. If Software was provided for limited term use, this Agreement will automatically expire at the end of the authorized term. Upon any termination or expiration, you agree to cease all use of Software and return it to Mentor Graphics or certify deletion and destruction of Software, including all copies, to Mentor Graphics' reasonable satisfaction.

10. **EXPORT**. Software is subject to regulation by local laws and United States government agencies, which prohibit export or diversion of certain products, information about the products, and direct products of the products to certain countries and certain persons. You agree that you will not export in any manner any Software or direct product of Software, without first obtaining all necessary approval from appropriate local and United States government agencies.

11. **RESTRICTED RIGHTS NOTICE**. Software has been developed entirely at private expense and is commercial computer software provided with RESTRICTED RIGHTS. Use, duplication or disclosure by the U.S. Government or a U.S. Government subcontractor is subject to the restrictions set forth in the license agreement under which Software was obtained pursuant to DFARS 227.7202-3(a) or as set forth in subparagraphs (c)(1) and (2) of the Commercial Computer Software - Restricted Rights clause at FAR 52.227-19, as applicable. Contractor/manufacturer is Mentor Graphics Corporation, 8005 Boeckman Road, Wilsonville, Oregon 97070-7777 USA.

12. **THIRD PARTY BENEFICIARY**. For any Software under this Agreement licensed by Mentor Graphics from Microsoft or other licensors, Microsoft or the applicable licensor is a third party beneficiary of this Agreement with the right to enforce the obligations set forth in this Agreement.

13. **CONTROLLING LAW**. This Agreement shall be governed by and construed under the laws of Ireland if the Software is licensed for use in Israel, Egypt, Switzerland, Norway, South Africa, or the European Union, the laws of Japan if the Software is licensed for use in Japan, the laws of Singapore if the Software is licensed for use in Singapore, People's Republic of China, Republic of China, India, or Korea, and the laws of the state of Oregon if the Software is licensed for use in the United States of America, Canada, Mexico, South America or anywhere else worldwide not provided for in this section

14. **SEVERABILITY**. If any provision of this Agreement is held by a court of competent jurisdiction to be void, invalid, unenforceable or illegal, such provision shall be severed from this Agreement and the remaining provisions will remain in full force and effect.

15. **MISCELLANEOUS**. This Agreement contains the entire understanding between the parties relating to its subject matter and supersedes all prior or contemporaneous agreements, including but not limited to any purchase order terms and conditions, except valid license agreements related to the subject matter of this Agreement which are physically signed by you and an authorized agent of Mentor Graphics. This Agreement may only be modified by a physically signed writing between you and an authorized agent of Mentor Graphics. Waiver of terms or excuse of breach must be in writing and shall not constitute subsequent consent, waiver or excuse. The prevailing party in any legal action regarding the subject matter of this Agreement shall be entitled to recover, in addition to other relief, reasonable attorneys' fees and expenses.